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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Jack H. Yuan et al.		
Title:	Non-Volatile Memory Cell Array Having Discontinuous Source and Drain Diffusions Contacted by Continuous Bit Line Conductors and Methods of Forming		
Application No.:	Unassigned	Filing Date:	Herewith
Examiner:	Unassigned	Group Art Unit:	Unassigned
Docket No.:	SNDK.217US2	Conf. No.:	Unassigned

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicants call the documents listed on the enclosed Form PTO-1449 to the Examiner's attention in this patent application. Copies of the documents listed on the accompanying Form PTO-1449 that are not enclosed were previously submitted in Application Nos. 09/667344 and 10/265,066, from which this Application claims an earlier effective filing date.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge

Attorney Docket No.: SNDK.217US2


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any fee that may be required, or to credit any overpayment, against Deposit Account No. 502664.

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EV437667592US

Respectfully submitted,



Gerald P. Parsons
Reg. No. 24,486

April 12, 2004

Date

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(415) 693-0194 (fax)

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-10317-1D US		Unassigned	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
(Use several sheets if necessary)					Jack H. Yuan and Jacob Haskell			
COPY					Filing Date		Group	
					Herewith		Unassigned	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	A1	4,336,603	Jun. 22, 1982	Kotecha et al.				
	A2	4,380,057	Apr. 12, 1983	Kotecha et al.				
	A3	4,417,264	Nov. 22, 1983	Angle				
	A4	4,477,825	Oct. 16, 1984	Yaron et al.				
	A5	4,855,955	Aug. 8, 1989	Cioaca				
	A6	4,885,719	Dec. 5, 1989	Brahmbhatt				
	A7	5,021,999	Jun. 4 1991	Kohda et al.				
	A8	5,043,940	Aug. 27, 1991	Harari				
	A9	5,047,362	Sep. 10, 1991	Bergemont				
	A10	5,070,032	Dec. 3, 1991	Yuan et al.				
	A11	5,095,344	Mar. 10, 1992	Harari				
Foreign Patent Documents								
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		Document	Date	Country	Class	Subclass	Yes	No
	B1	55-43862	Mar. 27, 1980	Japan				Abs
	B2	0 051 158 B1	Oct. 5, 1981	Europe				
	B3	58-222561	Dec. 24, 1983	Japan			X	
	B4	WO 95/19047	Jul. 13, 1995	PCT				
	B5	07-226449	Aug. 22, 1995	Japan				Abs
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	C1	Alberts and Kotecha, "Multi-Bit Storage Fet Earom Cell", IBM Technical Disclosure Bulletin, Vol. 24, No. 7A, Dec. 1981, pp. 3311-3314.						
	C2	Kamiya et al., "EPROM Cell With High Gate Injection Efficiency", Int'l Electron Devices Meeting Technical Digest, 1982, pp. 741-744.						
	C3	Pein and Plummer, "Performance of the 3-D Sidewall Flash EPROM Cell", Int'l Electron Devices Meeting Technical Digest, 1993, pp. 2.1.1-3.5.4.						
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

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	A12	5,095,461	Mar. 10, 1992	Miyakawa et al.					
	A13	5,159,570	Oct. 27, 1992	Mitchell et al.					
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	A15	5,210,047	May 11, 1993	Woo et al.					
	A16	5,278,439	Jan. 11, 1994	Ma et al.					
	A17	5,297,148	Mar. 22, 1994	Harari et al.					
	A18	5,313,421	May 17, 1994	Guterman et al.					
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	A27	5,492,846	Feb. 20, 1996	Hara					
	A28	5,576,567	Nov. 19, 1996	Mori					
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	B6								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
	C4	Ma et al., "A Dual-bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single-Vcc High Density Flash Memories", Int'l Electron Devices Meeting Technical Digest, 1994, pp. 3.5.1-3.5.4.							
	C5	Kuo et al., "TEFET - A High Density, Low Erase Voltage, Trench Flash EEPROM, 1994 Symposium on VLSI Technology, pp. 51-52.							
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	A29	5,606,521	Feb. 25, 1997	Kuo et al.					
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							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
	B7								
	B8								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
	C6	PCT International Search Report, International Application No. PCT/US01/29405, Apr. 12, 2002, 3 pages.							
Examiner			Date Considered						
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10/265,066

Applicant(s)/Patent Under
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YUAN ET AL.

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Thao P Le

Art Unit

2818

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6091633	07-2000	Cernea et al.	365.185.13
	B	US-6373095	04-2002	Bracchitta et al.	257/316
	C	US-6492228	12-2002	Gonzalez et al.	438/257
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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	S					
	T					

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